REMARKS

This communication is filed in response to the Office Action mailed on March 26, 2004. Claims 20 and 43 are amended; no claims are canceled; claims 5-6, 8-11, 19, 21-27, 31-33, 39-40, and 42 have been withdrawn; and no claims have been added. As a result, claims 1-65 remain pending in this Application.

Claims Objections

Objections to claims 20 and 43 were raised based on informalities. These have been modified as suggested in the Office Action, so as to correct typographical errors, and not for reasons related to patentability. It is respectfully noted that claim 43 has been amended to depend from pending claim 38, and is thus also to be considered as pending in this Application, rather than withdrawn.

§112 Rejection of the Claims

Claims 2-4, 28-30, and 34-37 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-4, 20, 28-30, and 34-38 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Because a *prima facie* case of lack of written description has not been established, nor has a *prima facie* case of indefiniteness been established, the Applicant respectfully traverses these rejections.

With respect to claims 2-4 and 45, it is asserted in the Office Action that the specification does not properly describe the "first and second conductive layers are power and ground planes of the circuit board" or "a circuit board having a power plane … ground plane …", and that the drawings do not show these features, or that such features need further definition in the specification and drawings. It is respectfully noted that these features are already specifically described in the Application at Pg. 10, lines 27-30, with respect to Figures 4A and 4B:

> "… the first conductive layer 110 may be a first power plane layer of the circuit board 100. Similarly, the second conductive layer 120 may be a second power plane layer of the circuit board 100. Alternatively, the second conductive layer 120 may be a ground plane of the circuit board 100."

A similar reference is made in the Application at Page 5, lines 4-8:

> "The circuit board includes at least two conductive layers formed around a dielectric, or insulating layer. … The conductive layers may be power planes, ground planes, or any combination of the two."

Thus, it is believed that claims 2-4 and 45 comply with the written description requirement of 35 USC § 112, first paragraph.

With respect to claims 28 and 34, it is asserted in the Office Action that the specification does not properly describe "a capacitor having a dielectric layer …", and that this limitation should be clarified in the specification and the drawings. It is respectfully noted that these features are specifically described in the Application at Pg. 9, lines 3-6:

> "Thus, a capacitor is formed between the two conductive layers. It is the degree and type of engagement between the two conductive layers, as well as the type of material selected to make up the dielectric layer inserted between them, that determines the ultimate capacitance of the resulting structure."

This structure is clearly illustrated in Figure 4A, wherein the conductive layers 110, 120, as well as the dielectric 130 between them, is shown. Capacitor 95 is specifically referenced at Pg. 10, line 10, and shown in Figure 4A. Thus, it is believed that claims 28 and 34 also comply with the written description requirement of 35 USC § 112, first paragraph.

It should be noted that "An application need not contain a word-for-word description of the claimed invention to satisfy the written description requirement. … All that is needed is that the application reasonably convey the claimed subject matter." *See* Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 738, 2002.

To make out a prima facie case of lack of written description, four elements must be shown:

1) The application does not reasonably describe or convey the concepts
2) to one of ordinary skill in the art
3) at the time of filing the patent application
4) of the claimed invention.

It is respectfully noted that "[i]f even one of these elements of the prima facie case is not present, the rejection is improper and must be withdrawn." *Id.* Since "[t]he initial burden is on the PTO to establish that the now claimed subject matter is not described by the specification …", the Office must show why this element is not sufficiently described in the application as to each element of the prima facie case. *Id.*, citing *Ex parte Anderson*, 21 USPQ 2d 1241 (B.P.A.I. 1991). Since such a showing has not been made, and since the construction of circuits boards having power planes, ground planes, and capacitors are indeed described and illustrated in the written description and figures as filed, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

It is asserted in the Office Action, with respect to the rejection under 35 USC § 112, second paragraph, that the phrase "… including a second interstice engaged with a first interstice and a dielectric layer disposed between the first and second interstices" is not understood with respect to claims 1, 20, 28, 34, and 38. While the Applicant appreciates the suggestion by the Examiner to re-word the claim, the Applicant also respectfully declines to take advantage of this offer since the Application clearly describes the claimed construction, both in the text and in the drawings, with respect to the engaged interstices 150, 160 and the dielectric layer 130. For example, at Pg. 9, lines 9-13, with respect to Figure 4A, the Application text is as follows:

> "… there is a first conductive layer 110 having an interstice 160 formed in it. The second conductive layer 120 has a second interstice 150 formed in it. The two interstices 150, 160 are engaged, or sinuously intertwined. However, between the engaged interstices 150, 160 a dielectric layer 130 is disposed."

Thus, it is believed that the text of claims 1, 20, 28, 34, and 38 complies with the written description requirement of 35 USC § 112, second paragraph.

The question is asked, with respect to claim 20, if the Applicant means "a first interstice has a plurality of first widths, which are the same or different widths"? The Applicant

apologizes for the confusion with respect to the text of the claim, and respectfully notes that the language of the claim has been amended to correct the typographical errors and clarify that the first interstice has a "plurality of widths laying in a first plane", and that the "second interstice has a single second width laying in a second plane".

As noted in the Application at Pg. 18, lines 1-17, with respect to Figure 14:

> "... the first interstice 150 has a plurality of first widths W3 laying in the first plane. The second interstice 160 has a complementary plurality of second widths W4 laying in the second plane. It should be noted that the side view of the configuration illustrated in Figure 14 is identical to that shown in Figure 13, such that the edges of the first and second planes 153 and 163 are substantially parallel with each other. However, in this case, each one of the first plurality of widths W3 substantially overlaps at least one of the second plurality of widths W4. Thus, in this manner, a multiplicity of vertically-overlapping capacitors, or capacitances, may be formed into the circuit board 100 to which the integrated circuit, memory module, or processor 330 is connected so as to form the circuit 101. ... the widths W3 and W4 are shown to be substantially overlapping. ... While the plurality of widths W3 and W4 are shown to be roughly similar in size in Figure 14, there is no absolute requirement that this be so. In fact, the designer of the circuit board 100 may select widths W3 and W4 to be any size that serves the purposes of a particular design according to the performance requirements of the circuit 101."

This should make it clear that the widths W3 and W4 can be selected to be the same size, or a different size. There may be multiple widths, as shown for widths W3 and W4, or there may be single widths, as shown in Figure 12, using widths W1 and W2, which may span the entire width of the circuit board 100. Thus, any number and combination of widths is possible.

It is also asserted in the Office Action that the phrase "a second conductive layer including a second interstice, and the second interstice has a second width" has no support in the specification or drawings with respect to claim 20. It is respectfully noted that the Application clearly describes the claimed construction, both in the text and in the drawings, with respect to the engaged interstices 150, 160 and the dielectric layer 130. For example, at Pg. 9, lines 9-13, with respect to Figure 4A, the Application text is as follows:

> "... there is a first conductive layer 110 having an interstice 160 formed in it. The second conductive layer 120 has a second interstice 150 formed in it. The two interstices 150, 160 are engaged, or sinuously intertwined. However, between the engaged interstices 150, 160 a dielectric layer 130 is disposed."

Thus, it is believed that the text of claim 20 is fully supported by the Application text and figures, and therefore complies with the written description requirement of 35 USC § 112, second paragraph.

The question is asked, with respect to claims 36 and 37, how it is possible to have a "pre-selected amount of capacitance" considering the dielectric constant of the dielectric layer? Questions regarding support for this aspect of various embodiments in the Application text and drawings were also raised. In response, the Applicant respectfully notes the text of the Application at Pg. 24, lines 1-9, with respect to Figure 18:

> "... the degree or amount of overlap between one or more sets of interstices may also be chosen to provide a preselected amount of capacitance ... between the first and second conductive layers. This ... may be used to provide a fine adjustment of the capacitance ... in addition to that provided by selecting a particular dielectric constant, or to adjust for dielectric materials of inconsistent or highly variable dielectric constants, or even to provide localized areas of greater or lesser capacitance for a circuit board design in order to accommodate varying signal speeds and characteristics which may arise in different locations of the board."

This should make it clear that the overlap of the widths of various interstices, along with selecting a particular material for the dielectric can operate to provide a preselected capacitance between the conductive layers. Thus, it is believed that the text of claims 36 and 37 also complies with the written description requirement of 35 USC § 112, second paragraph.

In addition, it is respectfully noted with respect to claims 1-4, 20, 28-30, and 34-38 that "[in] relation to Section 112, second paragraph, the Examiner has the burden of showing that the proposed claim language is indefinite to one of skill in the art." *Id.* at pg. 831. This type of showing has not been made.

To make out a *prima facie* case of indefiniteness, three elements must be shown:

1) interpretation of the claim in light of the specification;

2) interpretation of the claim as one of ordinary skill in the art would interpret it; and
3) that the limitation(s) in the claim, or the subject matter not in the claim, does not reasonably define the invention.

It is respectfully noted that "[a]n Examiner must clearly define the problem and why it is a problem in connection with the issue of claim definiteness in order to provide an applicant or any reviewing authority with the information necessary to evaluate the Examiner's position fairly." *Id.* at pg. 832. Nothing has been stated by the Office in this regard with respect to the claim language proffered by the Applicants. Since a *prima facie* case of indefiniteness has therefore not been established, and since the language of the claims is definite in light of the specification, it is respectfully requested that the rejection under 35 USC § 112, second paragraph, be reconsidered and withdrawn.

§102 Rejection of the Claims

Claims 1-4, 28, 38, and 65 were rejected under 35 USC § 102(b) as being anticipated by Nakao et al. (U.S. Patent No. 5,926,377, hereinafter "Nakao"). First, the Applicant does not admit that Nakao is prior art, and reserves the right to swear behind this reference in the future. Second, because Nakao does not disclose the identical invention as claimed, the Applicant respectfully traverses this rejection.

Nakao teaches a multilayer circuit board having capacitors 4 formed at the edges of an overlapping pattern of a power source layer 2 and ground layer 3. See Nakao, FIG. 1(a) and Col. 2, lines 39-53. The capacitors may be formed using electrodes 50, 51 protruding from the power source layer 2 toward the ground layer 3 and electrodes protruding form the edges of the ground layer 3 toward the power source layer 2. See Nakao, FIG. 16(b) and Col. 2, line 66 – Col. 3, line 4. The Office Action asserts that the electrodes 50, 51 of Nakao are the same as the interstices 150, 160 of claims 1-4, 28, 38, and 65. However, such is not the case.

Claim 1, directed to a circuit board, includes the following limitation: "a second conductive layer including a second interstice engaged with the first interstice". Thus the first and second interstices are designed to be *engaged* (see Figure 4A, elements 150, 160). To be "engaged" means "meshed," which, in turn, means "interlocked." *See Webster's Ninth New Collegiate Dictionary*, G. & C. Merriam Company, pgs. 412 and 744, 1983. In other words, if

one were to attempt to "pull" the conductive layers 110, 120 apart in the ±Y direction in Figure 4A, for example, the engaged interstices would prevent such separation. However, this cannot be said about the electrodes 50, 51 of Nakao. These electrodes, which are mere protusions from the surface of the power source and ground layers 23, 25, are not engaged. See Nakao, Col. 8, lines 12-16, and FIG. 16(b).

It is respectfully noted that anticipation under 35 USC § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *See Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added). Since Nakao does not teach engagement of the conductive layers, what is disclosed by Nakao is not identical to the subject matter of the embodiments claimed, and therefore, the rejection of claims 1-4, 28, 38, and 65 under § 102 is improper. Reconsideration and allowance are respectfully requested.

§103 Rejection of the Claims

Claims 29-30 were rejected under 35 USC § 103(a) as being unpatentable over Nakao in view of Novak (U.S. Patent No. 6,215,372, hereinafter "Novak"). Claims 34-37 were rejected under 35 USC § 103(a) as being unpatentable over Nakao in view of Lee et al. (U.S. Patent No. 5,497,037, hereinafter "Lee"). Claims 45-48 were rejected under 35 USC § 103(a) as being unpatentable over Nakao in view of Takeshita et al. (U.S. Patent No. 6,469,259, hereinafter "Takeshita"). First, the Applicant does not admit that Novak, Lee, or Takeshita are prior art and reserves the right to swear behind these references in the future. Second, since a *prima facie* case of nonobviousness has not been established, as required by M.P.E.P. § 2142, the Applicant respectfully traverses these rejections.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

No proper *prima facie* case of obviousness has been established because none of the required elements has been demonstrated, that is: (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

The References Do Not Contain All Limitations: First, with respect to independent claims 28, 34, 38, and 45-46, it has been demonstrated above that Nakao does not teach *engaged* conductive layers. Neither does Novak, Lee, or Takeshita.

Therefore, no combination of Nakao and Novak (or Lee or Takeshita) can provide the engaging conductive layers claimed by the Applicant in independent claims 28, 34, 38, and 45-46, and a *prima facie* case of obviousness has not been established. It is respectfully noted that if an independent claim is nonobvious under 35 USC § 103, then any claim depending therefrom is also nonobvious. See M.P.E.P. § 2143.03. Therefore all of the rejected dependent claims (i.e., claims 29-30, 35-37, and 47-48) are also nonobvious.

No Motivation to Combine the References: Combining Nakao and Novak does nothing to enhance or achieve the goals of either invention. In fact, Novak teaches away from such a combination, noting that "if ... the dielectric constant of dielectric layer 412 is increased in order to ...increase charge storage ... the increased dielectric constant ... capacitively loads the signal trace ... increase[ing] the signal propagation time and creat[ing] distortion." See Novak, Col. 17-26. This information, taken directly from Novak, is in direct contrast to the assertion made in the Office Action, that "it would have been obvious ...to use a dielectric layer ... as taught by Novak ... for the purpose of ... increasing charge storage in the dielectric layer." One of skill in the art would not be motivated to combine these references, since distorted signals are not a desired result. Thus, the Examiner appears to be using personal knowledge, and is therefore respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Similar difficulties exist with the proposed combination of Nakao and Lee, or Nakao and Takeshita. While the assertion is made that it "would have been obvious to ... utilize two power supplies in the system of Nakao et al., as taught by Lee et al. ... for the purpose of providing DC/DC or DC/AC voltage power, no such need is expressed by Nakao. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); and M.P.E.P. 2143.01. Thus, the assertion is not in accordance with the requirements of *In re Sang Su Lee*, and the Examiner appears to be using personal knowledge. It is therefore respectfully requested that the Examiner submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Finally, Takeshita also teaches away from such a combination, specifically disclaiming the approach taken by Nakao, as follows:

> "... the method of providing the capacitor to the outer circumference of the board ... demands a capacitor of a specific shape ... this poses a problem that the cost is increased by the capacitor or the productivity is reduced ..." See Takeshita at Col. 1, lines 61-67.

Thus, there is no motivation to combine Nakao with Novak, Lee, or Takeshita.

No Reasonable Expectation of Success: Adding the capacitors of Novak (or the power supplies of Lee, or the circuit elements of Takeshita) to the circuit board of Nakao does nothing

to ensure that the conductive layers disclosed by Nakao will be engaged as a result. This is because none of the references teaches the engaging structures described, illustrated, and claimed by the Applicant.

With respect to the combinations suggested in the Office Action, it is respectfully noted that the test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02.

In summary, none of the references teach the engagement of conductive layers as claimed by the Applicant in independent claims 1, 20, 28, 34, 38, and 44-46. No evidence has been entered in the record to support a need to combine the references (in fact the references teach away from these combinations), and no reasonable expectation of success results from any combination. The requirements of *M.P.E.P.* § 2142 have not been satisfied, and a *prima facie* case of obviousness has not been established with respect to these independent claims. All rejected dependent claims are also nonobvious, since claims depending from nonobvious independent claims are also nonobvious. It is therefore respectfully requested that the rejections to claims 29-30, 34-37, and 45-48 under 35 U.S.C. § 103 be reconsidered and withdrawn.

CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney, Mark Muller, at (210) 308-5677, or the undersigned, to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

STEVE VAN KIRK

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 28 June '04

By ______________________
Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28 day of June, 2004.

Tina Kohout

Name

Signature